Submicron InP–InGaAs Single Heterojunction Bipolar Transistors With f_T of 377 GHz

Walid Hafez, Jie-Wei Lai, and Milton Feng, *Fellow, IEEE*

***Abstract*—Submicron InP–InGaAs-based single heterojunction bipolar transistors (SHBTs) are fabricated to achieve record-breaking speed performance using an aggressively scaled epitaxial structure coupled with a submicron emitter process. SHBTs with dimensions of 0.35 $\times$16 μm have demonstrated a maximum current gain cutoff frequency f_T of 377 GHz with a simultaneous maximum power gain cutoff frequency $f_{\rm MAX}$ of 230 GHz at the current density Jc of 650 kA/cm^2. Typical $\rm BV_{CEO}$ values exceed 3.7 V.**

***Index Terms*—Heterojunction bipolar transistors (HBTs).**

I. Introduction

THE high-frequency performance of InP-based heterojunction bipolar transistors (HBTs) has steadily increased over the last few years. While double heterojunction transistors (DHBTs) have received much attention recently, InGaAs-based DHBT devices require complicated grading schemes to overcome current blocking at the base-collector junction [1]–[4], and high-quality GaAsSb material [5] is still difficult to obtain. In this paper, we report the fastest bipolar transistor to date using a simplistic SHBT layer structure. The submicron emitter dimensions allow for low-power operation while maintaining excellent dc characteristics. Such devices are critical to support high-speed low-power applications, such as 40-Gb/s OEIC receivers [6], [7] and analog-to-digital converters.

II. Layer Structure

The epitaxial structure used in this work was directed toward achieving high current cutoff frequencies (f_T) by scaling the layer thicknesses and high-power cutoff frequencies $(f_{\rm MAX})$ by a submicron lateral scaling process. The wafers were grown on Fe-doped semi-insulating (100) InP substrates by MBE. The layer structure is scaled from the previously reported University of Illinois at Urbana–Champaign (UIUC) structure in [6], [8]. The emitter doping level is increased to reduce emitter parasitic resistances and enhance current injection efficiency. The structure also employs a 300-Å compositionally graded base with an Indium mole fraction of 0.5 to 0.53 and C-doped ($p = 5 \times 10^{19}$ cm^{-3}, $R_{\rm sb} = 970\ \Omega/$sq) grown on a 1500-Å InGaAs collector. The design of the material structure has been specialized for UIUC submicron processing.

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The authors are with the Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801 USA.

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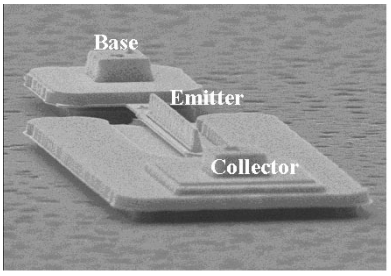

Fig. 1. Fabricated 0.35-μm $\times$ 8 μm InP–InGaAs SHBT before planarization.

III. Fabrication

The high-frequency devices were fabricated using a standard mesa process, utilizing both electron-beam and optical contact lithography. The process features an airbridge (referred to as a μ bridge in this work) to isolate the base terminal from the active device, thereby drastically reducing extrinsic parasitic capacitances. The fabrication relies exclusively on wet etching to achieve the undercutting desired to allow both the self-aligned base metal and the μ-bridge release.

Hexagonal emitters were defined using a Leica/Cambridge EBMF 10.5 e-beam system, resulting in a minimum emitter footprint of 0.35 μm. The undercut during the emitter-base etch was precisely controlled to within 60 nm. The self-aligned base metal pattern was also e-beam defined, and a 650-Å Ti–Pt–Au base metal stack was then deposited by e-beam evaporation. The use of such thin base metal did not adversely affect the mechanical robustness of the μ bridge. The devices are electrically isolated while simultaneously releasing the μ bridge and then planarized and encapsulated with bizbenzocyclobutene (BCB). The cured BCB provides structural support to the μ bridge during subsequent high-temperature processing steps. An etchback using a reactive ion etch (RIE) is then performed to expose the base, emitter, and collector terminals. NiCr resistors for on-wafer calibration are thermally deposited, followed by e-beam deposition of the overlay RF pads. An SEM image of a fabricated 0.35$\times$8 μm device before planarization is shown in Fig. 1.

IV. DC Results

Typical values of dc gain vary from 25 to 40 between 1 μA and 1 mA, with β remaining constant at 40 above 1 mA. Base and collector ideality factors are 1.35 and 1.18, respectively. A common emitter family of curves is shown in Fig. 2, where the collector–emitter offset voltage $V_{\rm CE,offset}$ is approximately 0.17 V and the knee voltage is less than 0.7 V. The common-emitter breakdown voltage $\rm BV_{CEO}$ is approximately 3.8 V for

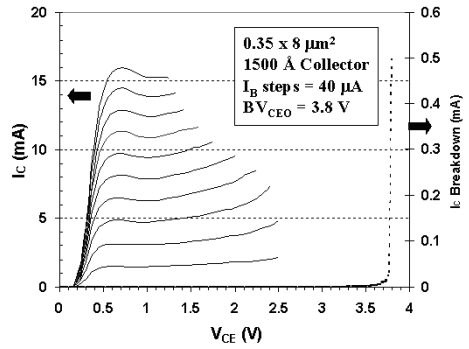

Fig. 2. Family of curve plots for a 0.35 $\times 8$ μm device.

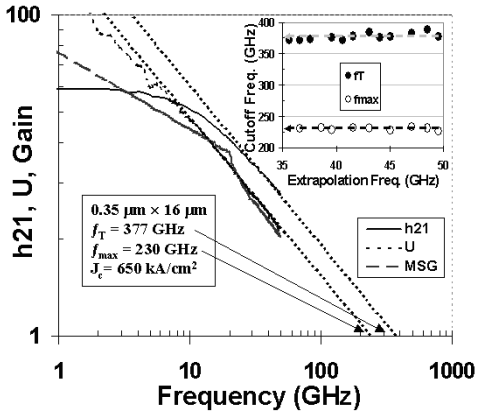

Fig. 3. Extrapolation of h_{21}, U, and MSG and f_T, $f_{\rm MAX}$ versus extrapolation frequency.

the 0.35×8 μm^2 device, and the avalanche breakdown at the peak f_T collector current is 2 V.

V. RF Results

The HBTs were characterized with an HP8510C network analyzer from 0.5 to 50 GHz. The calibration was performed with on-wafer short-open-load-thru (SOLT) standards. The current gain, Mason's unilateral gain, and MSG/MAG for a 0.35×16 μm^2 HBT are shown in Fig. 3. The cutoff values were obtained by averaging the -20 dB/decade extrapolations from 35 to 50 GHz. The dependence of f_T and $f_{\rm MAX}$ versus extrapolation frequency is shown in the inset of Fig. 3. The peak RF performance yields an f_T of 377 GHz and occurs at an Ic of 31 mA, corresponding to a Jc of 650 kA/cm^2 when device undercutting is factored into the emitter area calculation. An $f_{\rm MAX}$ of 230 GHz was achieved simultaneously at a $V_{\rm CB}$ of 0 V. Fig. 4 shows the cutoff frequencies versus collector current for various $V_{\rm CB}$ voltages. At $V_{\rm CB}$ of 0.1 V, the peak values for f_T and $f_{\rm MAX}$ are 368 and 238 GHz respectively, showing a weak dependence of the collector-base voltage on RF performance. We have also measured several HBTs with different emitter length as shown in Table I. For a 0.35×8 μm^2 HBT, an f_T of 370 GHz with associated $f_{\rm MAX}$ of 280 GHz was achieved. An alternative layout for the 0.35×8 μm^2 HBT, featuring a narrower base metal finger, yielded an f_T of 363 GHz with associated $f_{\rm MAX}$ of 310 GHz.

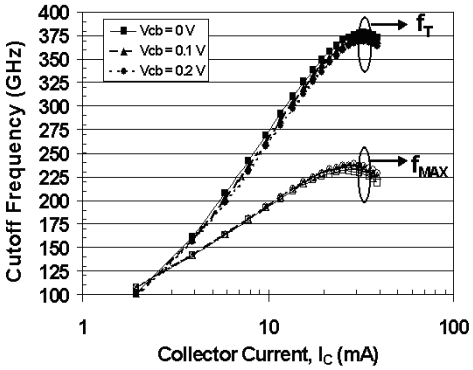

Fig. 4. f_T and $f_{\rm MAX}$ and versus collector current for various $V_{\rm CB}$ voltages.

TABLE I
PERFORMANCE SUMMARY FOR CURRENT BIPOLAR TECHNOLOGIES

Source	f_T (GHz)	f_{MAX} (GHz)	J_C (kA/cm^2)	β	W_E x L_E (μm^2)	BV_{CEO} (V)
HRL InP SHBT	180	220	250	30	0.5 x 4	2
SFU InP DHBT	300	300	410	45	0.4 x 11	6
NTT InP DHBT	341	238	833	34	0.8 x 3	2
IBM SiGe 9HP	350	170	2000	2300	0.12 x 2.5	1.4
UIUC InP SHBT-1	363	310	667	40	0.35 x 8	3.7
UIUC InP SHBT-2	370	280	683	40	0.35 x 8	3.8
UIUC InP SHBT-3	377	230	650	40	0.35 x 16	4.1

A summary of the characteristics of the most recent high-speed bipolar transistor is shown in Table I. The $f_T * {\rm BV_{CEO}}$ product for the UIUC devices exceeds 1550 GHz $\cdot$ V, well above the Johnson limit of 200 GHz $\cdot$ V [9]. In comparison, the UIUC InP–InGaAs SHBT surpass the best reported SiGe HBT (490 GHz $\cdot$ V) [10], InAlAs–InGaAs SHBT (360 GHz $\cdot$ V) [11] and InP–InGaAs DHBT(682 GHz $\cdot$ V) [1] and approach the latest InP–GaAsSb DHBT (1800 GHz $\cdot$ V) [5].

Transistor model parameter extraction was performed to better understand the dominant delay terms limiting the device speed. The major delay terms are as follows: $\tau_F = 0.35$ ps, (kT/Ic)Cje $= 0.056$ ps, $(kT/Ic)C_{\rm BC} = 0.023$ ps, $R_E C_{\rm BC} = 0.027$ ps and $R_B C_{\rm BC} = 0.20$ ps. These equivalent circuit parameters confirm the dominant delays are due to the forward transit time, τ_F, and the base-collector charging capacitance, $R_B C_{\rm BC}$.

VI. Conclusion

This paper has demonstrated superior dc and RF characteristics for SHBTs. The aggressive scaling of the epitaxial structure coupled with submicron emitter dimensions has produced record current gain cutoff frequencies. The RF performance along with the high-breakdown voltages exceeding 3.7 V suggest that SHBT devices will be important for low-voltage low-power mixed signal circuit applications.

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