Ultra High-Speed InP–InGaAs SHBTs With $f_{\max}$ of 478 GHz

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***Abstract*—InP-based single heterojunction bipolar transistors (SHBTs) for high-speed circuit applications were developed. Typical common emitter dc current gain (β) and $\mathrm{BV_{CEO}}$ were about 17 and 10 V, respectively. Maximum extrapolated $f_{\max}$ of 478 GHz with f_T of 154 GHz was achieved for 0.5 × 10 μm^2 emitter size devices at 300 kA/cm^2 collector current density and 1.5 V collector bias. This is the highest $f_{\max}$ ever reported for any nontransferred substrate HBTs, as far as the authors know. This paper highlights the optimized conventional process, and the authors have great hopes for the process that offers inherent advantages for the direct implementation to high-speed electronic circuit fabrication.**

***Index Terms*—Base-collector capacitance, base resistance, heterojunction bipolar transistors (HBTs), high-speed devices.**

I. Introduction

ONE OF the merits of InP-based HBTs is high speed and the HBTs have been used extensively for applications in fiber optical and wireless communication systems. We have developed the single HBT (SHBTs) for the purpose of high speed. Much effort has been made to reduce the base collector capacitance C_{bc} and base resistance R_b of the HBT since $f_{\max} \simeq \sqrt{f_T/8\pi R_b C_{\mathrm{bc}}}$. Several process techniques to reduce R_b and C_{bc}, such as isolation implantation of the extrinsic base and collector region [1], laterally etched undercut [2], epi regrowth for the thick base layer [3], L-shaped base electrode [4], horseshoe-shaped layout [5], and transferred-substrate technique [6] have contributed to a remarkable improvement in device performance.

However, this paper emphasizes the practical implementation of conventional processes. The base resistance (R_b) was minimized by optimizing the base contact resistivity. To reduce C_{bc}, a base-pad-isolation structure was utilized, which can eliminate the capacitance at the base-pad area. Additionally, the emitter parasitic resistance and inductance were minimized by using emitter metal widening and air-bridge structures. These optimized conventional processes delivered extremely high-speed InP SHBTs.

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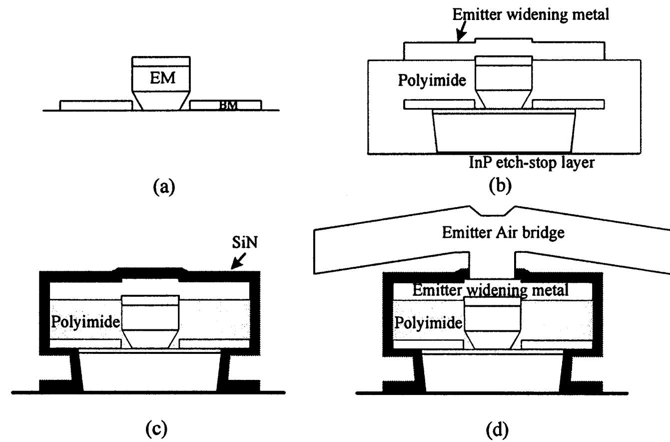

Fig. 1. Process flow (a) self-aligned base metal, (b) emitter metal widening, (c) SiN deposition, and (d) emitter air bridge.

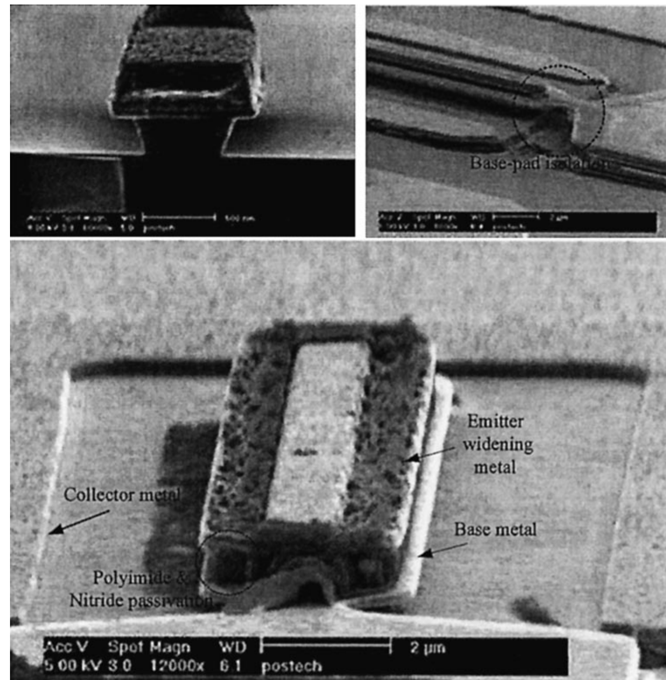

Fig. 2. SEM picture of the fabricated HBT with a 0.8 (effective 0.5) × 10 μm^2 emitter area.

II. Device Structure and Fabrication

The epitaxial layer of the fabricated HBTs is grown by IntelliEPI using Solid Source Molecular Beam Epitaxy (SSMBE) on an Fe-doped semi-insulating (100) InP substrate. The

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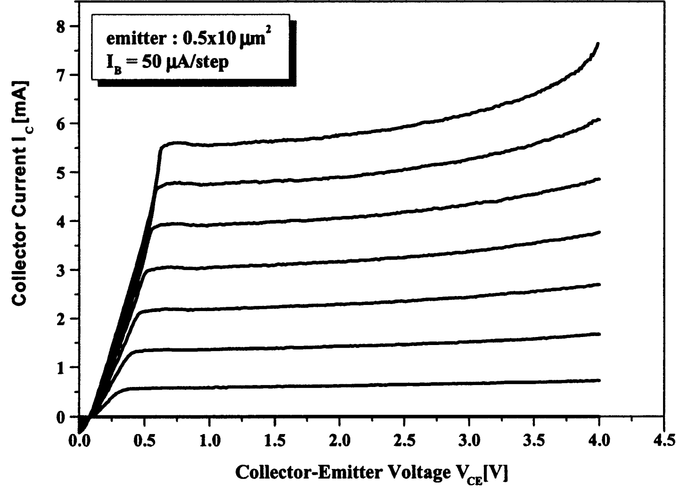

Fig. 3. Common emitter I_C–$V_{\rm CE}$ characteristics of the fabricated HBT with a 0.5 × 10 μm^2 emitter area.

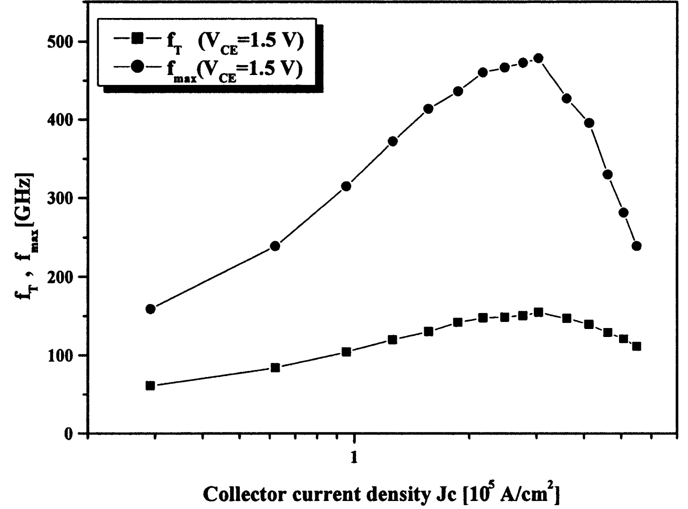

Fig. 4. Dependence of f_T and $f_{\max}$ on collector current density of the fabricated HBT with a 0.5 × 10 μm^2 emitter area.

layer structure includes, from the top, an InGaAs emitter contact layer, InGaAlAs graded layers, InP emitter (700 Å, Si-doped to 7.0 × 10^{17} cm^{-3}), InGaAs base (400 Å, C-doped to 6.0 × 10^{19} cm^{-3} with 20 Å spacer), InGaAs collector layer (4000 Å, Si-doped to 2.0 × 10^{16} cm^{-3}), and an InGaAs subcollector.

Fabrication started with the evaporation of the Ti–Pt–Au emitter contact metal having a width of 0.8 μm. Emitter etch, which is one of the most delicate steps, was carried out by the selective etch of citric-based and subsequent hydrochloric-based wet processes, and the emitter was slightly undercut, resulting in an effective 0.5-μm size. After the emitter etch, a self-aligned Pt–Ti–Pt–Au base metal with a width of 1 μm was evaporated [Fig. 1(a)]. The emitter was protected by photo-resist using a base contact mask and the base and collector layers were then etched with a citric-based etchant. Next, Polyimide was coated and then flatly etched without a mask using an O_2 RIE until the emitter metal was exposed. Next, a Ti–Au emitter widening metal was evaporated [Fig. 1(b)], and second, the polyimide etch was performed until the epilayer was exposed. Next, SiN was deposited. The SiN was mask etched and the residual polyimide was removed by ashering [Fig. 1(c)] [7]. The subcollector was etched for device isolation. In this etching process, the active base area and the base pad area for interconnection were isolated. Next, Ti–Pt–Au collector metal and pad metal were evaporated. Lastly, Au air-bridge formation followed [Fig. 1(d)]. SEM pictures of the fabricated HBTs are shown in Fig. 2. For high-speed InP HBTs, the emitter and base metal widths were 0.8 (effectively 0.5 μm) and 1 μm. The base-to-emitter spacing measured from the SEM picture was about 0.15 μm.

III. Device Measurement Results

I–V curves of the fabricated HBTs with 0.5×10 μm^2 emitter area are measured and are depicted in Fig. 3. As shown, the common-emitter dc current gain (β) of the fabricated HBTs is about 17 at a collector current density of 1 × 10^5 A/cm^2. Breakdown voltages of the fabricated HBTs at an open base, $\mathrm{BV_{CEO}}$ is very high, about 10 V. Base sheet resistance ($R_{\rm SB}$) of 560 Ω/□ and specific contact resistivity ($\rho_{\rm BC}$) of

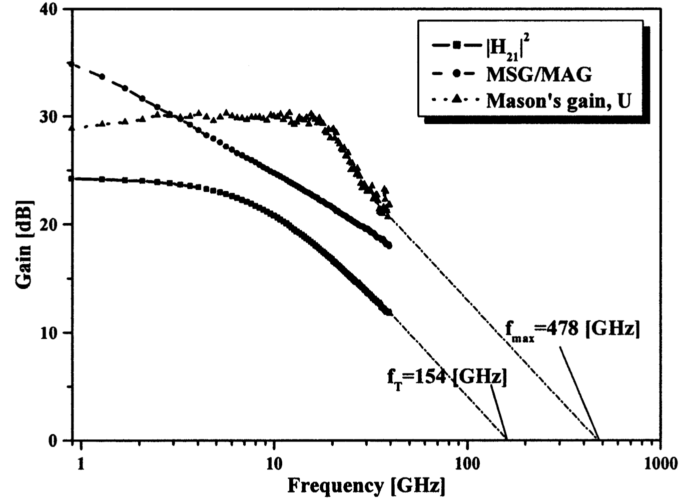

Fig. 5. Frequency dependencies of $|h_{21}|^2$, MSG/MAG, and Mason's gain (no pad-deembedding).

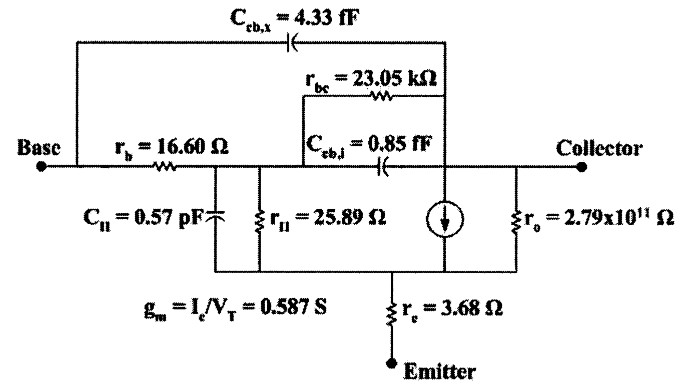

Fig. 6. Small-signal equivalent circuit model at $I_C = 15.2$ mA and $V_{\rm CE} = 1.5$ V.

2.5 × 10^{-7} Ω·cm^2 are measured using Transmission Line Measurement (TLM). The transfer length L_T, expressed as $(\rho_{\rm BC}/R_{\rm SB})^{1/2}$, is 0.21 μm and the base contact resistance is maintained low.

The microwave performance of the fabricated HBTs is characterized by on-wafer S-parameter measurements from 0.5 to 40 GHz using a Agilent 8510C network analyzer calibrated by thru-reflect-line (TRL) method. f_T and $f_{\max}$ are estimated assuming a -20 dB/decade frequency dependence of the current gain and Mason's unilateral gain, respectively. Fig. 4 shows the dependence of f_T and $f_{\max}$ on collector current density at 1.5 V collector bias. Frequency dependencies of the current gain, Mason's unilateral gain, and maximum stable gain/maximum available gain are shown in Fig. 5. f_T and $f_{\max}$ of the HBT are 154 and 478 GHz ($\mathrm{Gain} \simeq 21.7$ dB at 40 GHz), respectively, at $I_C = 15.2$ mA and $V_{\mathrm{CE}} = 1.5$ V. To our knowledge, this is the highest $f_{\max}$ ever reported for any nontransferred substrate HBTs.

From the measured S-parameters, small-signal model parameters of the device are extracted and are shown in Fig. 6. Despite the conventional structure, the time constant $R_b C_{\mathrm{bc},i}$ is evaluated to be very low, about 14.11 fs. This is due to the low base contact resistance, since the transfer length (L_T), expressed as $(\rho_{\mathrm{BC}}/R_{\mathrm{SB}})^{1/2}$ ($\simeq$0.21 μm), remains shorter than the effective base width ($\simeq$1 μm), although the base layer is attacked during the base and collector layer etchings. Also, the extrinsic base collector capacitance $(C_{\mathrm{cb},x})$ is very low, 4.33 fF, since the base-pad is isolated. The emitter resistance (r_e) is maintained low by using the emitter metal widening and air-bridge structures even though the emitter width is small, about 0.5 μm. These improved structure results in the very high-speed HBT.

IV. Conclusion

High-speed InP–InGaAs SHBTs are fabricated by using the POSTECH process. The processes include good base ohmic contact, base-pad isolation, emitter metal widening, and air-bridge structures. High-frequency performance of $f_T = 154$ GHz and $f_{\max} = 478$ GHz is obtained from the HBT with a 0.5×10 $\mu\mathrm{m}^2$ emitter area. This is the highest $f_{\max}$ ever reported for any nontransferred substrate HBTs. This conventional process can be a practical technique for implementation to high-speed electronic circuits. Also, as the device is scaled down, the device RF performance will be further improved.

Acknowledgment

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