InP/InGaAs SHBTs with 75 nm collector and $f_T > 500$ GHz

W. Hafez, Jie-Wei Lai and M. Feng

InP/InGaAs single heterojunction bipolar transistors (SHBTs) are fabricated exhibiting current-gain cutoff frequencies, f_T of 509 GHz. The $0.35 \times 12\ \mu m^2$ devices consist of a 25 nm graded base and a 75 nm collector, have a breakdown BV_{CEO} of 2.7 V, and operate at current densities above 1100 kA/cm². This work demonstrates clear progress toward a THz transistor.

Introduction: Efforts to improve f_T are focusing on the reduction of electron transit time by vertically scaling the base and collector thicknesses at the cost of increasing base-collector parasitic capacitance [1–6]. An estimated 75% of the total delay time comes from the electron transit time, therefore, transit time reduction is a very efficient way to boost device speed through vertical scaling. It is well understood that the improvement in f_T from vertical scaling comes at the expense of a reduction in f_{MAX} and breakdown voltage. To compensate the drop in f_{MAX}, lateral scaling of the device dimensions must be employed to facilitate transistors with sufficiently high speeds to be useful in circuit applications. This Letter demonstrates vertically and laterally scaled HBT devices achieving state-of-the-art performance of $f_T = 509$ GHz, the fastest bipolar transistor reported to date.

Device layer structure and fabrication: The layer structure used in the fabrication of these devices is a scaled extension of the structure detailed in [2]. The epitaxial structure consists of a 300 nm subcollector Si doped at $n = 4 \times 10^{19}\ cm^{-3}$, a 75 nm collector doped at $n = 1 \times 10^{16}\ cm^{-3}$, a 25 nm compositionally graded base (0.53 to 0.50 Indium grading) Carbon doped to $p = 6 \times 10^{19}\ cm^{-3}$, and a 40 nm emitter cap with a doping of $n = 4 \times 10^{19}\ cm^{-3}$. The base sheet resistance is measured to be 1030 Ω/square, as determined from TLM measurements.

Fabrication follows a standard triple mesa, all wet-etch process previously detailed in [7, 8]. The primary reason for the achievement of simultaneously high f_T and f_{MAX} values in these devices is attributed to the use of a metal bridge, referred to as a μ-bridge, which is undercut to eliminate the parasitic base to collector capacitance associated with the large base contact post. The process flow includes e-beam defined Ti/Pt/Au emitter contacts, a self-aligned emitter etch, a self-aligned Ti/Pt/Au base metal deposition, a base–collector etch, and collector metal deposition. A bisbenzocyclobutene (BCB) based etch-back process is employed for device planarisation and back end fabrication.

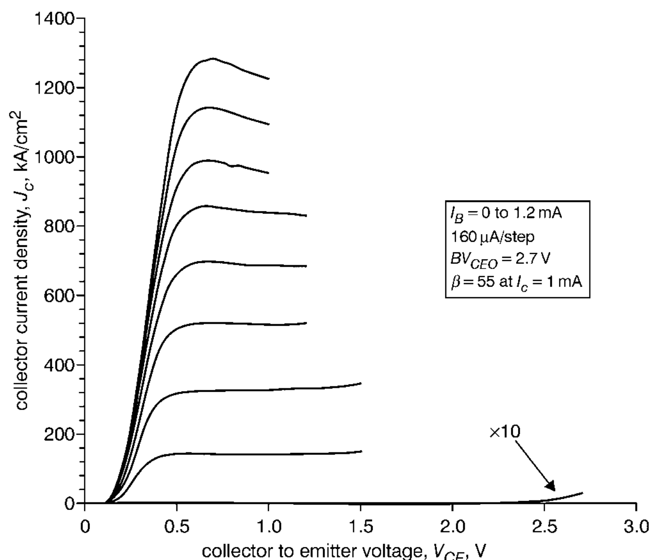

Fig. 1 *Common collector output characteristics for $0.35 \times 12\ \mu m^2$ device*

Device results: Fig. 1 shows common-emitter output characteristics for a $0.35 \times 12\ \mu m^2$ HBT. The current gain, β, for the devices varies with collector current; values range from 50 at $I_C = 0.5$ mA to 68 at $I_C = 25$ mA. Junction ideality factors are 1.34 and 1.14 for the base and collector, respectively. The breakdown for this device is measured at approximately $BV_{CEO} = 2.7$ V as shown in Fig. 1. This breakdown value, however, can be misleading, as the breakdown under operating conditions is much lower. It is important to note the presence of thermal effects around the peak f_T operating current of this device ($I_C = 47.2$ mA, $V_{BE} = 0.94$ V); thermal pulldown and gain compression at high current levels are, along with Kirk effect, the dominant mechanisms limiting the bandwidth of the devices.

The RF calibration was achieved using an on-wafer short-open-load-thru (SOLT) calibration, and S-parameters were obtained using an HP8510C from 50 MHz to 50 GHz. On-wafer calibration is preferred, as it requires no additional deembedding of dummy structures, which can create a significant source of error when removing parasitic pad capacitances that approach the same order of magnitude as device capacitances. The extrapolations were obtained by assuming a −20 dB/decade slope from the h_{21} and U curves, as shown in Fig. 2 for a $0.35 \times 12\ \mu m^2$ device. The extrapolated f_T and f_{MAX} values remained independent of extraction frequency out to 50 GHz, indicating that a good calibration was achieved. All RF measurements were carried out at a collector/base voltage $V_{CB} = 0$ V, which was shown to yield the highest f_T performance.

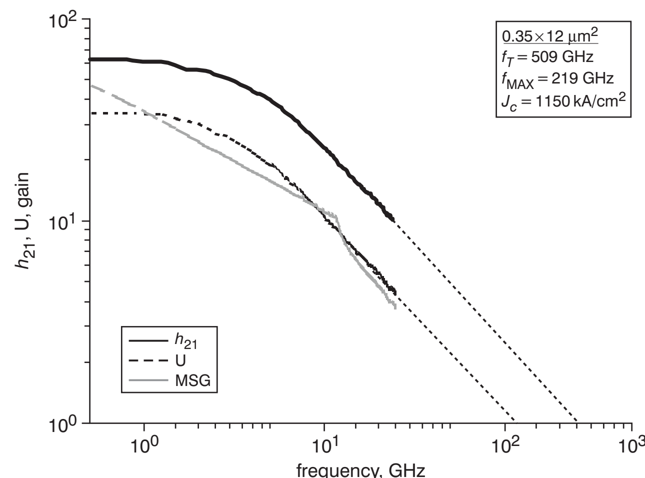

Fig. 2 *h_{21}, U and MAG/MSG extrapolation for $0.35 \times 12\ \mu m^2$ device, operating at $V_{CB} = 0$ V*

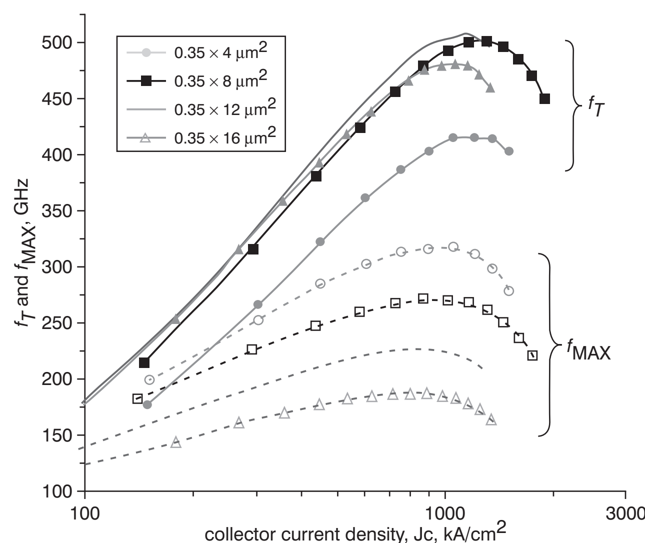

Fig. 3 *f_T and f_{MAX} against collector current density for multiple emitter length HBTs with 0.35 μm emitter widths*

Fig. 3 shows the cutoff frequency performance against collector current density for transistors with lengths of 4, 8, 12 and 16 μm, each with an emitter junction width of 0.35 μm. Peak performance was achieved at $f_T = 509$ GHz with a simultaneous $f_{MAX} = 219$ GHz at $J_C = 1150$ kA/cm² for the 12 μm device. The $0.35 \times 8\ \mu m^2$ devices achieve $f_T = 504$ GHz with $f_{MAX} = 261$ GHz. These devices reach peak

f_T at 36 mA, corresponding to a $J_C = 1300$ kA/cm^2. For the 0.35 × 4 μm^2 devices, f_T and f_{MAX} were 415 and 318 GHz, respectively. The reduction in f_T for the smaller device is attributed to an increase in emitter metal resistance. The observed increase in f_{MAX} for the shorter emitter lengths is due to a decrease in base metal sheet resistance from transmission line effects as previously observed in [7].

Conclusion: InP/InGaAs SHBTs were fabricated to achieve cutoff frequencies greater than 500 GHz using a self-aligned submicron process. The thin collector structure allows a reduction of transit time, as well as an increase in peak current density due to an extension of J_{Kirk}. The performance of these transistors is suitable for future high-speed applications, with increasingly higher speed and lower power operation expected as further device scaling is exploited.

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