Novel gate-recessed vertical InAs/GaSb TFETs with record high I_{ON} of 180 μA/μm at V_{DS} = 0.5 V

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Abstract

Vertical tunnel field-effect transistors (TFETs) in which the gate field is aligned with the tunneling direction have been fabricated using a novel gate-recess process, resulting in record on-current. The tunnel junction consists of InAs/GaSb with a broken band alignment. The gate-recess process results in low drain contact and access resistances; together with the favorable broken gap heterojunction, this leads to a record high I_{ON} of 180 μA/μm at V_{DS} = V_{GS} = 0.5 V with an I_{ON}/I_{OFF} ratio of 6×10^3. Both SiN_x passivation and forming gas anneal (FGA) were found to improve the device subthreshold swing (*SS*), resulting in a SS_{MIN} of 200 mV/dec at 300 K and 50 mV/dec at 77 K. Capacitance-voltage (*C-V*) measurements indicate that the device *SS* performance is limited by interfacial trap density (D_{it}).

Introduction

III-V TFETs with small effective mass and staggered or broken energy band alignments are promising for low power logic applications because of their potential for low *SS* and low voltage (V_{DD}) operation, while simultaneously maintaining sufficiently high I_{ON} and low I_{OFF} [1]. TFETs with broken gap tunnel junctions were only very recently demonstrated using InAsSb/GaSb nanowires prepared by bottom-up growth [2]. We have recently demonstrated a new geometry for TFETs, in which the tunneling direction is normal to the gate; these devices showed promising results but exhibited low I_{ON} limited by the drain contact [3]. In this paper, we report *n*-channel InAs/GaSb TFETs fabricated using a novel gate-recess process showing the highest I_{ON} at V_{DS} = 0.5 V among all *n*-TFETs demonstrated to date. Also investigated are the effects of passivation of etched undercuts and mesas by plasma-enhanced chemical vapor deposition (PECVD) SiN_x, FGA and the temperature dependence of device characteristics.

Device Structure and Fabrication

The interband tunnel junction consists of a 30 nm Si-doped *n*+ InAs contact layer (Si, 3.0 x 10^{19} cm^{-3}), a 1 nm undoped InP etch stop, 6 nm n-InAs channel (Si, 1.0 x 10^{17} cm^{-3}), 40 nm *p*+ GaSb source (Be, 4.0 x 10^{18} cm^{-3}) and 300 nm *p*+ GaSb buffer (Be, 5 x 10^{19} cm^{-3}) on a *p*+ GaSb substrate (Zn ~ 3 x 10^{18} cm^{-3}) (Fig. 1(a)). Fig. 1(b) outlines the process flow and Fig. 1(c) shows the TFET cross section. Device fabrication started with Ti/Au drain metallization and lift-off. PECVD SiN_x sidewalls were then formed around the drain by blanket deposition and anisotropic dry etch, followed by selectively etching of the 30 nm InAs contact layer in 1 H_2SO_4:8 H_2O_2:1000 H_2O (1-8-1000) to stop at the 1 nm InP, and atomic layer deposition (ALD) of a 0.7 nm Al_2O_3/ 4.5 nm HfO_2 gate dielectric (equivalent oxide thickness, EOT ~1.3 nm) at 300 °C right after the etching. Then, after Ti/Cr gate metallization by blanket e-beam evaporation, methyl methacrylate (MMA) planarization and etch back, Ti/Cr on top of the drain was etched using MMA as mask. Next, after MMA removal using acetone and benzocyclobutene (BCB) planarization and etch back, Ti/Cr and Ti/Au were deposited to define the gate open area and form the drain contact. BCB, Ti/Cr and high-*k* dielectrics were then etched sequentially outside of the device active area and the gate metal (Ti/Cr) was exposed after one more BCB etch. The 6 nm InAs layer was then selectively etched in 1-8-1000 to stop at the *p*+ GaSb source followed by a highly-selective GaSb etch (1 NH_4OH:1 H_2O) until the GaSb under the drain and the SiN_x spacer was removed to form an undercut mesa structure. 10 nm of SiN_x was deposited at 120 °C by PECVD to prevent atmospheric degradation of the thin exposed semiconductor layers under the gate and drain. Finally, FGA was applied at 250 °C for 20 mins by furnace annealing in 5% H_2/ 95% Ar.

Energy band diagrams of the transistor in operation are shown in Figs. 2(a) and (b). In the off state (V_{GS} = 0 V), the confinement causes the ground state energy E_1 in the 6-nm InAs to lie above the Fermi level on the *p*+ GaSb side (E_{fp}), leading to a low interband tunneling probability in the off state. When a positive gate voltage is applied (V_{GS} = 0.2 V), E_1 is below E_{fp} and the transistor is on. The as-grown and gate-recessed surfaces are smooth with an RMS roughness of 0.25 nm and 0.42 nm (Fig. 3(a) and (b)), respectively. A cross-sectional scanning electron micrograph (SEM), prepared by a focused-ion beam of a fabricated vertical TFET, Fig. 4(a), shows that the tunnel junction is fully overlapped by the gate electrode and therefore the current modulation observed in these TFETs is entirely due to gate control. The TEM image under the gate (Fig. 4(b)) confirms the thicknesses of the amorphous dielectrics (0.7 nm Al_2O_3 and 4.5 nm HfO_2) and InAs channel (6 nm). Fig. 4(c) focuses on the InAs drain contact, spacer, and recessed gate structure.

Layer description		
nm	material	cm^{-3}
30	n+InAs	3.E19
1	InP	undoped
6	n-InAs	1.E17
3	p-GaSb	undoped
47	p+GaSb	4E18
200	p+GaSb	5E19
p+GaSb substrate		

- ☐ Ti/Au drain formation
- ☐ SiN_x spacer formation
- ☐ InAs selective wet etch
- ☐ ALD high-k deposition
- ☐ Ti/Cr gate blanket deposition
- ☐ MMA etch back
- ☐ Dry etch Cr and wet etch Ti
- ☐ MMA removal
- ☐ BCB etch back
- ☐ Gate open area definition (Ti/Cr)
- ☐ Drain contact definition (Ti/Au)
- ☐ Etch BCB, Cr/Ti, high-k
- ☐ InAs and GaSb selective wet etch
- ☐ SiN_x passivation
- ☐ Forming gas annealing

(a) (b)

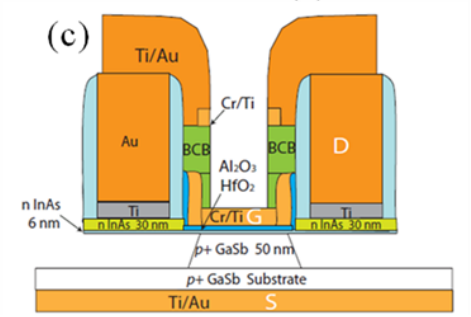

Fig. 1 Vertical InAs/GaSb TFET with the gate field and tunnel direction aligned: (a) layer description, (b) key process steps, and (c) device cross-section.

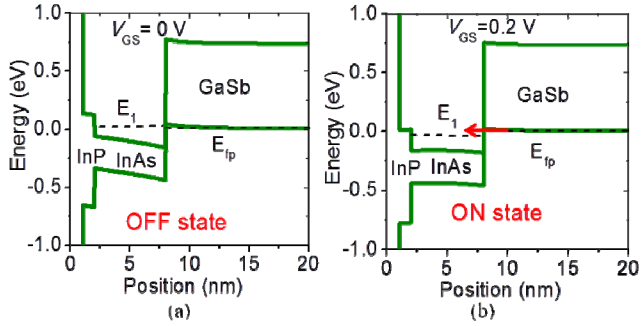

Fig. 2 (a) OFF and (b) ON-state energy band diagrams simulated using a self-consistent Schrodinger/Poisson solver.

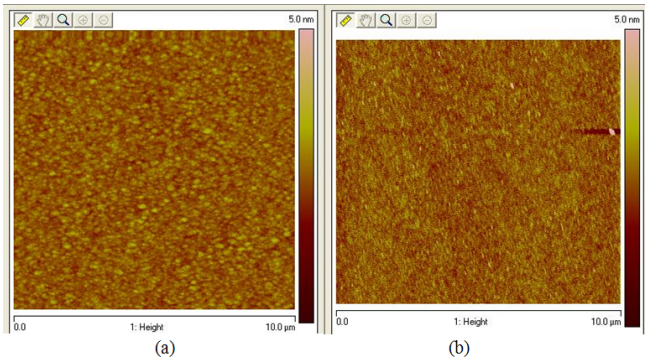

Fig. 3 Atomic force microscope (AFM) images of the surface (a) before and (b) after gate recess etching of the top 30 nm InAs contact layer. Root mean square (RMS) roughness is 0.25 nm and 0.42 nm, respectively.

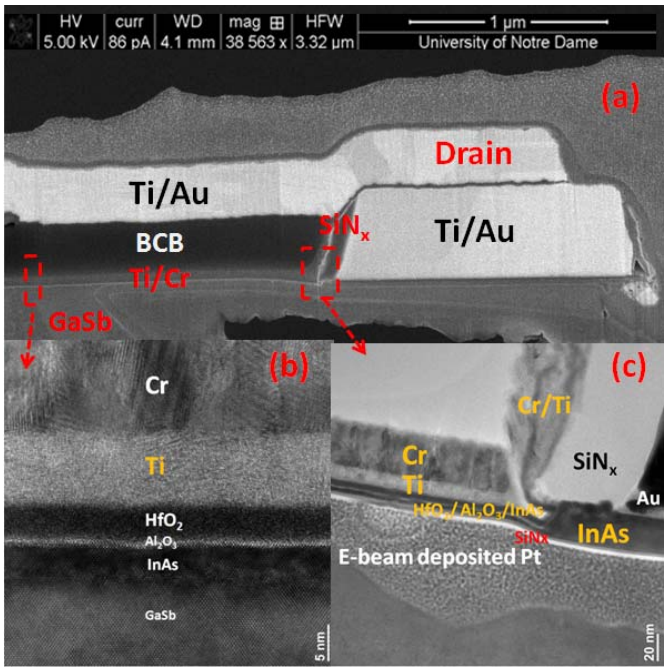

Fig. 4 (a) Cross-sectional SEM image of a fabricated vertical gate-recessed InAs/GaSb TFET. (b) TEM image of the gate dielectric and tunnel junction stack. (c) TEM image of the drain contact, recessed-gate, SiN_x drain spacer and passivation.

Device Characterization

Figure 5 shows the I_D–V_{DS} characteristics, at 300 K, of a TFET after FGA and SiN_x passivation (the gate area is 40×70 µm^2 and perimeter is 220 µm). Assuming the drain current is carried along all four edges of the gate, the calculated I_{ON} is 380 µA/µm at V_{DS} = V_{GS} = 1 V and 180 µA/µm at V_{DS} = V_{GS} = 0.5 V, a record high on-current for TFETs at these bias conditions, while the gate current is at least one order of magnitude smaller than the drain current. The high I_{ON} results from the significantly improved drain contact resistance (~100 -µm) due to the thick extrinsic drain enabled by the gate recess process and the InAs/GaSb tunnel junction, compared to previous reports [3]. The TFET has an I_{ON}/I_{OFF} of 6×10^3 over a gate swing of 1.5 V. The drain induced barrier thinning (DIBT) is also very small, < 80 mV/V. A SS_{MIN} of 200 mV/dec is achieved at both V_{DS} = 0.5 V and 1 V. The I_D–V_{DS} characteristics at 77 K (Fig. 6(a)) show that with the tunnel junction under forward bias (V_{DS} < 0), a clear trend toward negative differential resistance (NDR) is observed. For this device, the SS_{MIN} reduced from 200 mV/dec at 300 K to 50 mV/dec at 77 K, while the on current reduced by ~10% (Fig. 6(b) and 6(c)). This temperature dependence most probably results from reduced trap-assisted tunneling and increased bandgap at 77 K [3].

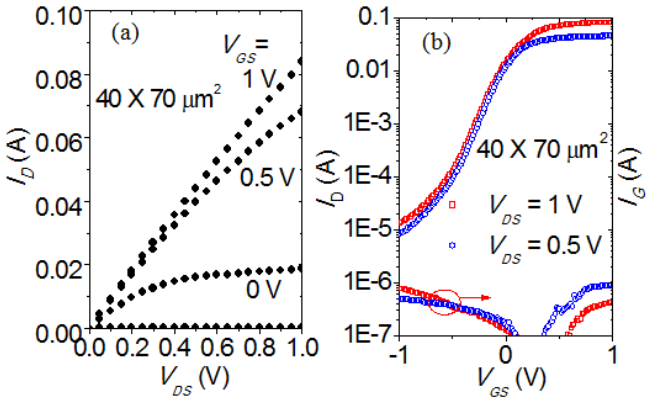

Fig. 5 (a) I_D–V_{DS} characteristics with V_{GS} varied from -1 to 1 V and a 0.5 V step. (b) Measured TFET log I_D and I_G vs. V_{GS} at V_{DS} = 0.5 and 1 V. An SS_{min} of 200 mV/dec is obtained.

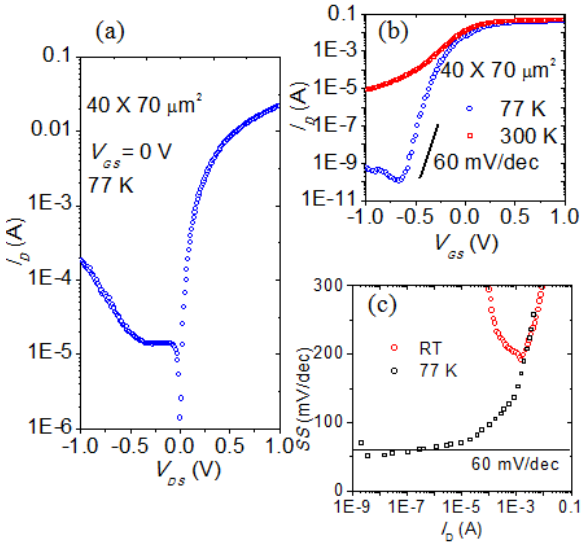

Fig. 6. Log I_D–V_{DS} characteristics with V_{GS} =0 V at 77 K. A trend toward NDR is observed in the forward-biased tunnel junction (V_{DS}<0). (b) Temperature dependent I_D–V_{GS} characteristics of a TFET after FGA and passivation. (c) Tangential subthreshold swing versus I_D and as a function of V_{DS}, showing that SS_{MIN} decreased from 200 mV/dec at 300 K to 50 mV/dec at 77 K at V_{DS} = 0.5 V.

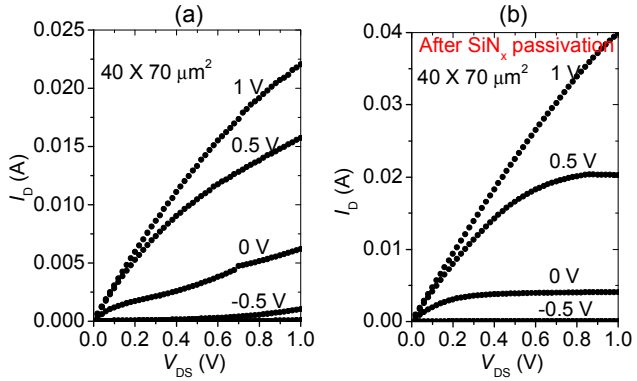

Fig. 7. Measured I_D–V_{DS} characteristics of a TFET at 300 K (a) before and (b) after SiN_x passivation.

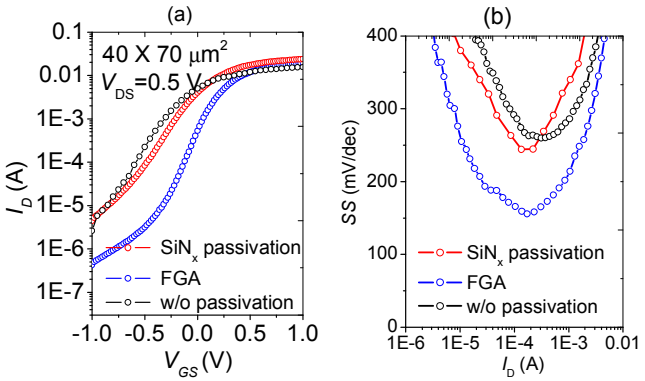

Fig. 8 (a) TFET log I_D vs. V_{GS} at V_{DS} = 0.5 V measured sequentially: as-fabricated, after SiN_x passivation, and after FGA. (b) Corresponding tangential *SS* versus I_D, showing the SS_{MIN} improvement with FGA and SiN_x passivation.

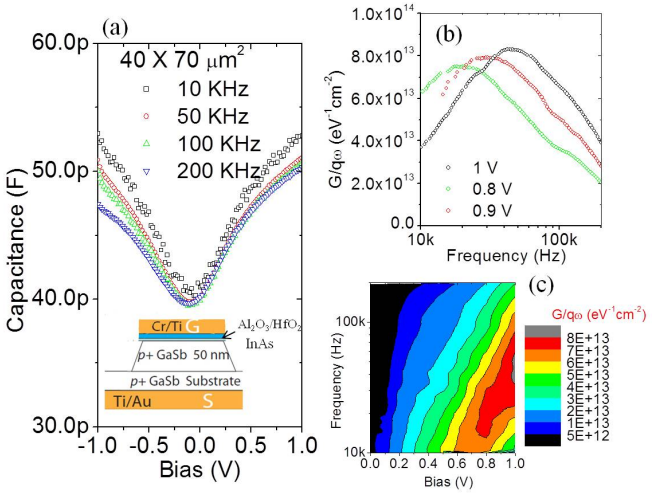

Fig. 9. Multi-frequency (10 kHz – 200 kHz) *C-V* (a) and *G-V* (b) characteristics of an HfO_2/Al_2O_3/InAs/GaSb MOS capacitor on the fully fabricated sample. The inset is the device cross section. (c) Normalized parallel conductance ($G/\omega q$) as a function of V_G and frequency at 300 K.

Another device on the same sample designed with a larger GaSb undercut was utilized to study the effect of SiN_x passivation and FGA. A larger GaSb undercut leads to an increase in parasitic access resistance and thus a decrease in I_{ON}, but with a concomitant improvement in electrostatics and *SS* [1]. As shown in Fig. 7, with SiN_x passivation, I_{ON} increased from 100 μA/μm to 180 μA/μm, at V_{DS} = V_{GS} = 1 V, and improved pinch off and saturation at high V_{DS} voltage were also observed. Fig. 8 shows the measured TFET I_D–V_{GS} transfer characteristics and the associated tangential *SS* at V_{DS} = 0.5 V at 300 K. With FGA, the SS_{MIN} is reduced from 250 mV/dec to 150 mV/dec and I_{ON}/I_{OFF} increases from 5×10^3 to 5×10^4, which is consistent with a reduction in D_{it} by FGA [4]. To assess the impact of D_{it}, multifrequency (10 kHz – 200 kHz) *C-V* and conductance-voltage (*G-V*) characteristics of an HfO_2/Al_2O_3/6-nm-InAs/GaSb MOS capacitor (MOSCAP) on the fully processed sample at 300 K are shown in Fig. 9(a) and 9(b). The *G-V* characteristics show

$(G/\omega q)_{peak} \sim 8\times10^{13}$ cm^{-2} eV^{-1} at $V_{GS} = 0.9$ V, corresponding to a $D_{it} \sim 2\times10^{14}$ cm^{-2} eV^{-1} near the InAs conduction band edge [5]. Fig. 9(c) shows the corresponding conductance map. The conductance peak moves to different frequencies with gate bias, indicating the Fermi level is not pinned despite the high D_{it} [5]. Also the decreasing $(G/\omega q)_{peak}$ with decreasing V_{GS} indicates D_{it} reduces toward the middle of the InAs bandgap. With reduction in the D_{it}, sub-60 mV/dec is achievable at 300 K using these TFET configurations [1, 9]. For comparison, Table I benchmarks the on current (I_{ON}), on-off ratio (I_{ON}/I_{OFF}), SS_{MIN} and SS_{EFF} of III-V TFETs demonstrated to date.

Conclusion

State-of-the-art III-V TFETs in the broken gap InAs/GaSb system have been demonstrated using a novel gate-recessed structure in conjunction with a TFET geometry with tunneling direction normal to the gate. Record on-current density is achieved.

Acknowledgement

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TABLE I
PERFORMANCE COMPARISON OF MEASURED III-V CHANNEL TFETS

	Source	Channel	Dielectric	EOT	I_{ON}	V_{DS}	$V_{GS}=V_{ON}$	$V_{ON}-V_{OFF}$	I_{ON}/I_{OFF}	S_{MIN}	S_{EFF}
				nm	μA/μm	V	V	V		mV/dec	mV/dec
this work	GaSb	InAs	Al_2O_3/HfO_2	1.3	380	1	1	2	7,500	200	520
this work	GaSb	InAs	Al_2O_3/HfO_2	1.3	180	0.5	0.5	1.5	6,000	200	400
Dey [2]	GaSb	InAsSb	Al_2O_3/HfO_2	2.3	110	0.3	1.5	3	275	300	1200
Zhou [3]	InP	InGaAs	Al_2O_3/HfO_2	1.3	20	0.5	1	1.75	450,000	93	310
Mohata [6]	$Al_{0.53}In_{0.47}As$	$GaAs_{0.35}Sb_{0.65}$	Al_2O_3/HfO_2	1.75	135	0.5	1	1.5	17,000	230	350
Zhao [7]	$In_{0.7}Ga_{0.3}As$	$In_{0.7}Ga_{0.3}As$	HfO_2	1.2	40	0.5	2	2	200,000	84	380
Mohata [8]	$GaAs_{0.35}Sb_{0.65}$	$In_{0.7}Ga_{0.3}As$	Al_2O_3/HfO_2	2	135	0.5	1.5	1.5	10	750	1500
Li[9]	$Al_{0.45}Ga_{0.55}Sb$	InAs	Al_2O_3/HfO_2	1.6	78	0.5	0.5	1.5	1,600	125	470
Dewey [10]	$In_{0.53}Ga_{0.47}As$	$In_{0.53}Ga_{0.47}As$	TaSiOx	1.1	5	0.3	0.8	0.9	70,000	58	190

S_{MIN} and S_{EFF} are the minimum and effective subthreshold swings respectively; $S_{EFF} = (V_{ON} - V_{OFF}) / \log(I_{ON}/I_{OFF})$ [11]

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